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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,515	09/28/2001	Tomoo Kimura	60188-101	2527

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EXAMINER
THOMPSON, ANNETTE M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)	
	09/964,515	KIMURA ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 9* is/are rejected.

7)☒ Claim(s) *4-8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicants' Amendment Under 37 C.F.R. § 1.111 has been examined. The abstract is amended. Claims 1-10 are amended. Claims 1-10 are pending.

1. Applicant's Amendment has been examined and remarks considered. However, it is not considered persuasive. The applicable objections and rejections of the prior office action are incorporated herein together with any current objections and rejections.

Claim Objections

2. Claims 1-10 are objected to because of the following informalities: Pursuant to claims 1-10, these claims recite instances of the phrase "semiconductor circuit to be verified" which creates an antecedent basis issue. Applicants should either delete the phrase "to be verified" or add *element* after "semiconductor circuit". Pursuant to claim 8, this claim recites the limitations "the same operation pattern" and "the same hierarchical state" in lines 5-6. There is insufficient antecedent basis for these limitations in the claims. Applicants must rephrase claim to accurately claim the subject matter of the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Rejection of Claims 1-3 and 9

5. **Claims 1-3 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tani, U.S. Patent 5,471,409. Tani discloses a logic simulator apparatus and a circuit simulator apparatus capable of simulation based on signal propagation delay time. Tani does not explicitly disclose a current density analysis. However, Tani suggests current density analysis or calculation by inclusion of the elements required for a current density analysis. As outlined in section 4 of the Jerke et al. paper entitled "Hierarchical Current Density Verification for Electromigration Analysis in Arbitrarily Shaped Metallization Patterns of Analog Circuits", cited here for evidentiary purposes only and not as prior art, "Any current density calculation method requires at minimum (1) a set of current values as boundary constraints, (2) an appropriate representation of the layout geometry (3) technology dependent data and (4) specified application data (e.g. average chip temperature or a temperature field plot)". Tani includes all of the elements (listed in the Jerke paper) necessary for a current density calculation and furthermore discloses current calculating (col. 4, ll. 31-34). It would have been obvious

to one of ordinary skill in the art at the time of Applicants' invention that Tani's current calculation includes or at least suggests the inclusion of current density calculation.

6. Pursuant to claim 1, which recites [a] circuit operation verifying method for verifying layout design specifications (col. 1, ll. 5-9) comprising loading condition information as electrical specifications on voltages and currents applied to the circuit elements (col. 2, line 50 to col. 3, line 33; col. 6, ll. 22-66), circuit diagram data representing connection information of the semiconductor circuit (col. 2, ll. 54-56; col. 8, ll. 13-21), and input patterns of voltages (col. 2, line 66 to col. 3, line 2; col. 3, ll. 18-25) and currents (col. 3, ll. 10-13; col. 4, ll. 30-33) used for circuit operation simulation; simulating operation of the circuit to be verified while computing voltage values (col. 4, ll. 21-29) or current values (col. 4, ll. 30-46; col. 5, line 65 to col. 6, line 5) with respect to time based on the loaded circuit diagram data and input patterns and storing the computed values in memory (col. 12, ll. 57-64); verifying that the circuit elements to be verified satisfy the loaded condition information using the stored voltage or current values (col. 5, ll. 3-17), said verification being performed concurrently with said simulating operation (col. 5, ll. 10-14).

7. Pursuant to claim 2, wherein the condition information includes electrical specifications representing current density values (col. 6, ll. 25-65) and heat generation amounts (col. 19, ll. 35-40) of the circuit elements, and the circuit diagram data of the semiconductor circuit to be verified includes layout information (col. 6, ll. 21-27), and current density analysis and heat generation analysis at positions inside the semiconductor circuit to be verified are performed based on the current values at the

circuit elements and the layout information stored in the memory (col. 6, line 63 to col. 7, line 2).

8. Pursuant to claim 3, wherein the condition information includes time specifications representing the frequency of violation against the electrical specification or the time period for which a violation state is allowable (col. 4, line 50 to col. 5, line 2), and whether or not the frequency of violation of the circuit elements to be verified satisfy the time specifications.(col. 4, line 30 to col. 5, line 14; see also col. 13, ll. 19-27; col. 14, ll. 37-55).

9. Pursuant to claim 9, which recites a circuit operation verifying apparatus (Fig. 21; col. 1, ll. 10-13) for verifying that each of a number of circuit elements satisfies specifications (col. 1, ll. 5-9); loading means for loading condition information as electrical specifications on voltages and currents applied to circuit elements ((col. 2, line 50 to col. 3, line 33; col. 6, ll. 22-66); circuit diagram data representing connection information of the semiconductor circuit (col. 2, ll. 54-56; col. 8, ll. 13-21); input patterns of voltages (col. 2, line 66 to col. 3, line 2; col. 3, ll. 18-25) and currents (col. 3, ll. 10-13; col. 4, ll. 30-33) used for circuit simulation with respect to time; and operation simulation means for simulating operation of the semiconductor circuit while computing voltage values (col. 4, ll. 21-29) or current values (col. 4, ll. 30-46; col. 5, line 65 to col. 6, line 5) with respect to time (col. 11, ll. 9-18); verification means for verifying that circuit elements to be verified satisfy the specifications in the loaded condition information using the voltage values or the current values at the circuit elements stored in the memory (col. 5, ll. 3-17; col. 9, ll. 14-18; see also col. 9, ll. 3-8), said verification means

performing said verification concurrently (col. 5, ll. 10-14) with said simulation means performing said simulating operation.

Allowable Subject Matter

10. Claims 4-8 and 10 contain allowable subject matter.

11. The following is a statement of reasons for the indication of allowable subject matter: In a circuit operation verifying method, *as claimed by Applicants*, the prior art does not teach or suggest the use of a waveform display apparatus. Additionally, the prior art does not teach or suggest the designation of a verification and a non-verification period. Further, the prior art does not teach or suggest circuit hierarchy.

Remarks

12. Applicants' amendment introduces the added limitation which recites "said verification being performed concurrently with said simulating operation." Applicants assert that support for this limitation may be found on page 14, line 15 to page 15, line 4 of Applicants' specification. It states in pertinent part,

> Thus, according to the present invention, during operation simulation of a semiconductor circuit to be verified, whether or not circuit elements constituting the semiconductor circuit to be verified satisfy voltage specifications or current specification ***is verified every time voltage or current computation results are stored in a memory*** at infinitesimal/ time intervals. Therefore, with the use of data stored in the memory that enables high-speed read/write, the condition verification of the semiconductor circuit to be verified can be executed at high speed, and this shortens the verification time. (emphasis added).

According to the cited passage, verification occurs subsequent to the results being stored in a memory; Applicants, however, use the term concurrent to define this process. The method of the '409 patent is at least as "concurrent" as Applicants'

method as verification occurs "while the logic simulation is performed" (column 5, lines 12-14). Therefore, the rejection of claims 1-3, and 9 are maintained.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703)306-3329.

15. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)
(703)872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Patent Examiner

8 July 2003

MATTHEW SMITH
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TECHNOLOGY CENTER 2800